What is claimed is:

1. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

a ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port; and

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means, whereby in detecting a presence of said electrostatic pulse said ESD pulse detection means generates a voltage that triggers said ESD pulse clamp means thereby shunting said electrostatic pulse from said IC.

2. The circuit of claim 1 wherein said ESD pulse detection means contains a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter.

3. The circuit of claim 2 wherein said voltage inverter comprises a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port.

4. The circuit of claim 3 wherein said first port of said voltage inverter is connected to said first terminal of said IC, while said second port of said voltage inverter is connected to said second terminal of said IC.

5. The circuit of claim 3 wherein said connections of gate of said PMOS device and of said NMOS device are commonly connected to said third port of said voltage inverter.

6. The circuit of claim 3 wherein said connection of drain and said connection of bulk of said PMOS device are commonly connected to said first port of said voltage inverter.

7. The circuit of claim 3 wherein said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter.

8. The circuit of claim 3 wherein said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter.

9. The circuit of claim 2 wherein said capacitive component has a first terminal and a second terminal, said first terminal of said capacitive component is connected to said first terminal of said IC, said resistive component has a first terminal and a second terminal, said second terminal of said resistive component is connected to said second port of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component are commonly connected to said third port of said voltage inverter.

10. The circuit of claim 1 wherein said ESD pulse clamp means comprises a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port.

11. The circuit of claim 10 wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate of said PMOS device is connected to said third port of said ESD pulse clamp means.

12. The circuit of claim 2 wherein said capacitive component of said ESD pulse detection means comprises:

a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive component; and

a NMOS device having connections of gate electrode, source, drain and bulk whereby said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component, said connection of source is

connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component.

13. The circuit of claim 2 wherein said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component.

14. The circuit of claim 2, wherein:

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive, said capacitive component further comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component,

said connection of source is connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component; and

said resistive component comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connection of gate is connected via a resistive load to said second terminal of said resistive component, said connection of source is connected to said second terminal of said resistive component, said connections of drain and of bulk are commonly connected to said first terminal of said resistive load.

15. The circuit of claim 2 wherein:

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component; and

said resistive component of said ESD pulse detection means comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connections of source and bulk of

said NMOS device are commonly connected to said second terminal of said resistive component, said connection of gate is connected via a resistive load to said first terminal of said capacitive component, said connection of drain of said NMOS device is connected to said first terminal of said resistive component.

16. The circuit of claim 10 wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said first port of said voltage inverter, said connection of gate of said PMOS device is connected to said third port of said voltage inverter, said connection of bulk of said PMOS device is connected to said connection of gate of said PMOS device via well resistance that is present in the N-well underlying said PMOS device.

17. The circuit of claim 16 wherein said capacitive component of said ESD pulse detection means comprises parasitic capacitance

that is present between said third port of said voltage inverter and said first terminal of said IC.

18. The circuit of claim 10 wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of bulk of said PMOS device to connected to said third port of said ESD pulse clamp means via well resistance that is present in a N-well underlying said PMOS device, said connection of source said PMOS device is connected to said first port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said second port of said IC, said connection of gate of said PMOS device is connected to said first port of said ESD pulse clamp means via a resistive load.

19. The circuit of claim 18 wherein said capacitive component of said ESD pulse detection means comprises parasitic capacitance that is present between said third port of said voltage inverter and said first terminal of said IC.

20. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component, a capacitive component, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage

inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connection of bulk and drain of said PMOS device is commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprising a first terminal and a second terminal, said first terminal of said capacitive component being connected to said first terminal of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

21. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage

inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive component, said capacitive component also comprising a NMOS device having connections of gate electrode, source, drain and bulk whereby said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component, said connection of source is connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said

capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

22. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from

potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said

NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk whereby said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component.

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second

port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

23. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said

first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of

said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive component, said capacitive component further comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component, said connection of source is connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component;

said resistive component comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connection of gate is connected via a resistive load to said second terminal of said resistive component, said connection of source is connected to said second terminal of said resistive

component, said connections of drain and of bulk are commonly connected to said first terminal of said resistive load; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate of said PMOS device is connected to said third port of said ESD pulse clamp means.

24. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to

extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said

voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter; said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component;

said resistive component of said ESD pulse detection means comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connections of source and bulk of said NMOS device are commonly connected to said second port of said resistive component, said connection of gate is connected via a resistive load to said first port of said capacitive component, said connection of drain of said NMOS device is connected to said first terminal of said resistive component; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second

port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

25. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said

first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of

said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprising a first terminal and a second terminal, said first terminal of said capacitive component being connected to said first terminal of said IC; and

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component of said pulse detector and said first terminal of said resistive component of said pulse detector being commonly connected to said third port of said voltage inverter; said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said first port of said voltage inverter, said connection of gate of said PMOS device is connected to said third port of said voltage inverter, said connection of bulk of

said PMOS device is connected to said connection of gate of said PMOS device via well resistance that is present in the N-well underlying said PMOS device.

26. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second

terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connection of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device is commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprising a first terminal and a second terminal, said first terminal of said capacitive component being connected to said first terminal of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of bulk of said PMOS device to connected to said third port of said ESD pulse clamp means via well resistance that is present in a N-well underlying said PMOS device, said connection of source said PMOS device is connected to said first port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said second port of said IC, said connection of gate of said PMOS device is connected to said first port of said ESD pulse clamp means via a resistive load.

27. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has

as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is

connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises parasitic capacitance that is present between said third port of said voltage inverter and said first port of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second port of said IC, and said first terminal of said being connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp

means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said first port of said voltage inverter, said connection of gate of said PMOS device is connected to said third port of said voltage inverter, said connection of bulk of said PMOS device is connected to said connection of gate of said PMOS device via well resistance that is present in the N-well underlying said PMOS device.

28. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said

first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of

said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises parasitic capacitance that is present between said third port of said voltage inverter and said first port of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said resistive component being connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of bulk of said PMOS device is connected to said third port of said ESD pulse clamp means via well resistance that is present in a N-well underlying said PMOS

device, said connection of source said PMOS device is connected to said first port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said second port of said IC, said connection of gate of said PMOS device is connected to said first port of said ESD pulse clamp means via a resistive load.